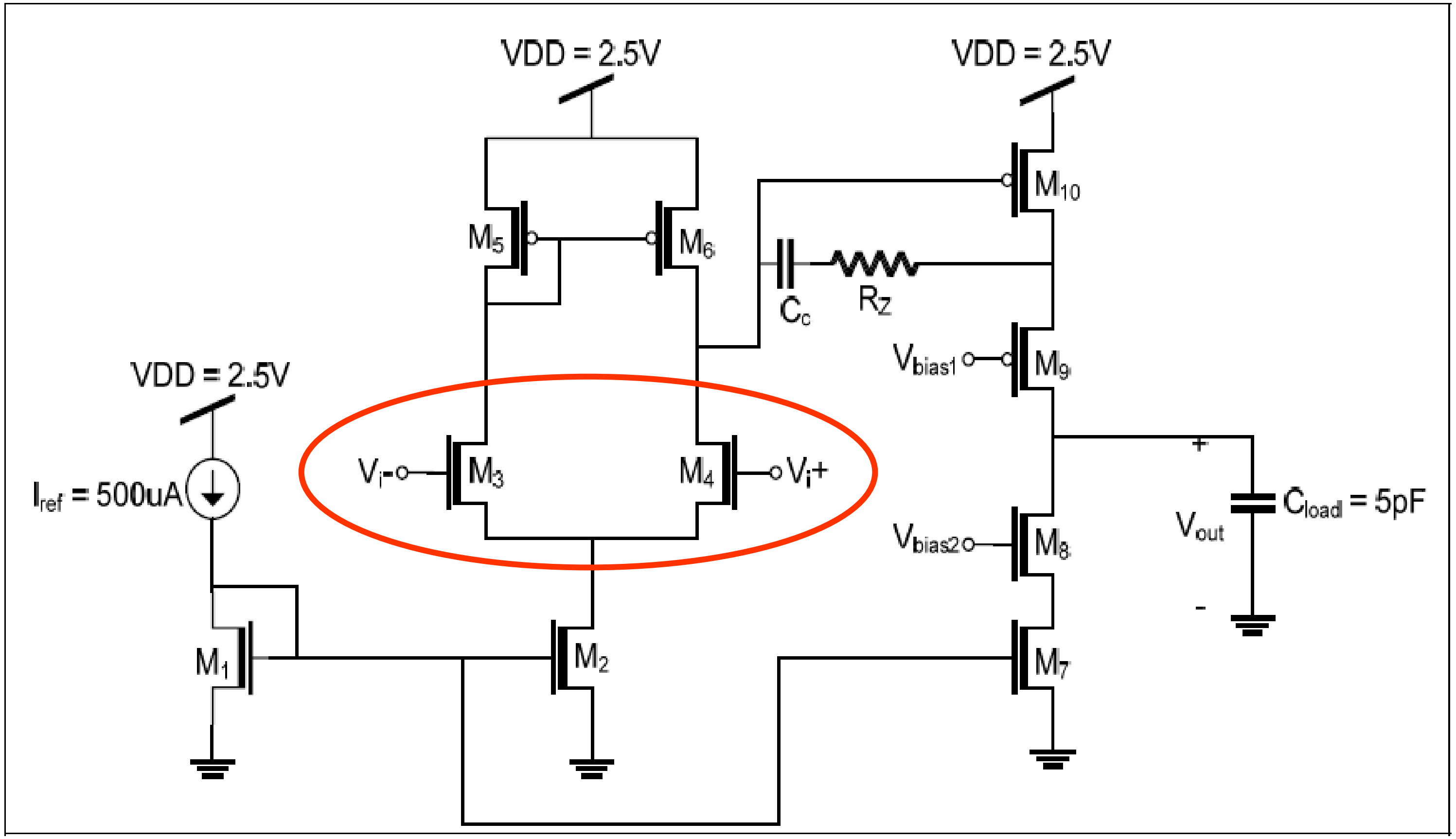
Lect. 11: Differential Amplifiers



<Fig. 2> 2-Stage OTA Schematic

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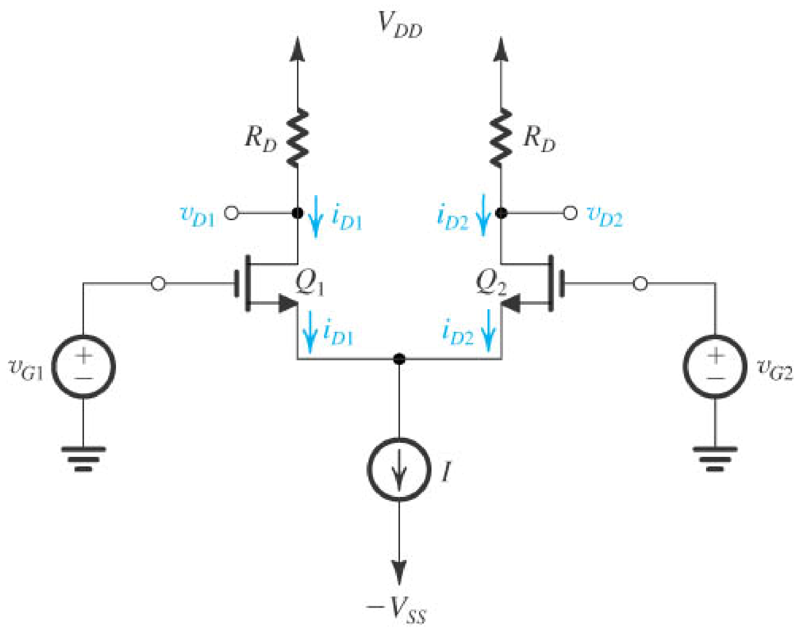
Differential Amplifier



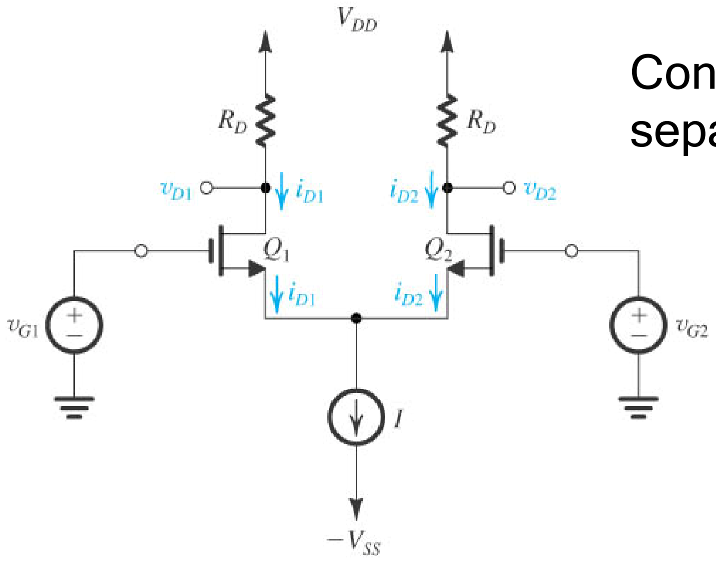
If $v_{G1} = v_{G2}$, $v_o = v_{D1} - v_{D2} = 0$

If $v_{G1} > v_{G2}$, $v_o < 0$

If $v_{G1} < v_{G2}$, $v_o > 0$

Non-zero output only for input difference
➔ Differential amplifier

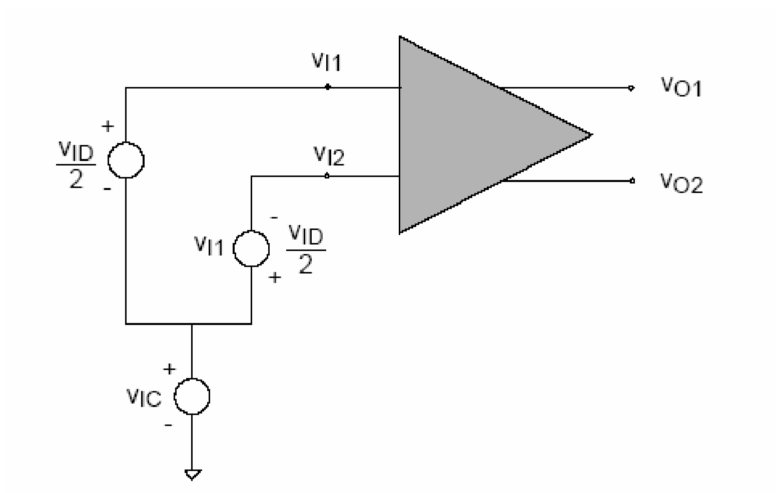
Lect. 11: Differential Amplifiers



Consider Common-Mode and Differential-Mode separately.

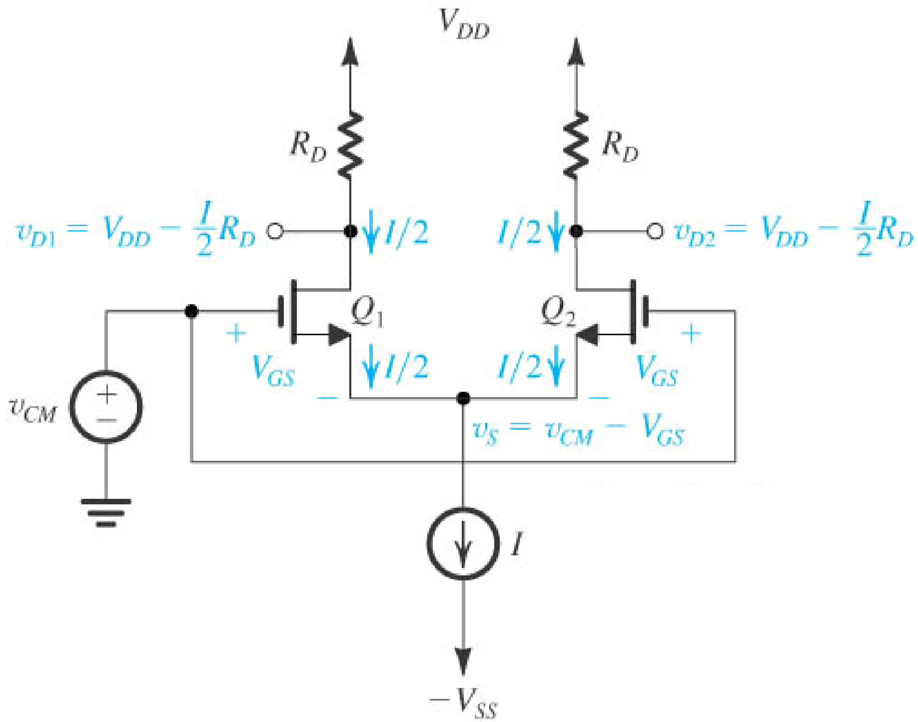
$$v_{G1} = V_{CM} + \frac{v_{id}}{2},\ v_{G1} = V_{CM} - \frac{v_{id}}{2}$$

$$V_{CM} = \frac{v_{G1} + v_{G2}}{2},\ v_{id} = v_{G1} - v_{G2}$$



Lect. 11: Differential Amplifiers

Common-Mode: $v_{G1} = v_{G2} = v_{CM}$



$$\upsilon_{D1} - \upsilon_{D2} = 0 \text{ (No CM output)}$$

$v_{CM,\ max}$?

$$v_{DS} \geq v_{GS} - V_t$$

$$(V_{DD} - \frac{I}{2}R_D) - (v_{CM} - v_{GS}) \geq v_{GS} - V_t$$

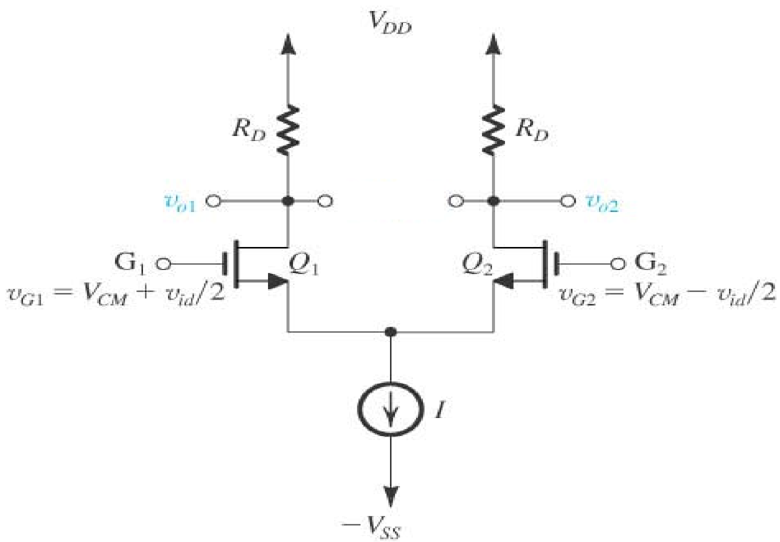
$$V_{DD} - \frac{I}{2}R_D + V_t \geq v_{CM}$$

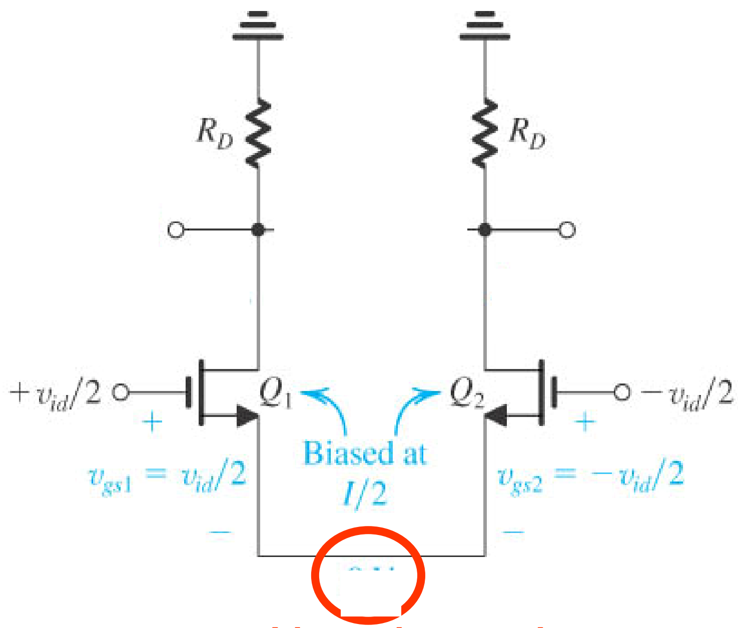
$$\therefore \upsilon_{CM,\max} = V_t + V_{DD} - \frac{I}{2}R_D$$

$v_{CM,\ min}$?

➔ Input common-mode range

Differential-mode small-signal analysis (assume $v_{id} < V_{CM}$)



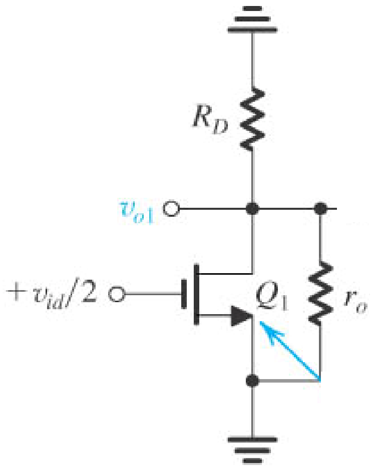


$$v_{od} = v_{o1} - v_{o2} = -g_m R_D \frac{v_{id}}{2} - g_m R_D \frac{v_{id}}{2} = -g_m R_D v_{id}$$

$$A_d = \frac{v_{od}}{v_{id}} = -g_m R_D$$

With r_o, $A_d = -g_m (R_D \| r_o)$

Differential-mode small-signal half-circuit ➔ Consider only half circuit



$$\frac{v_{o1}}{v_{id}/2} = -g_m(R_D \parallel r_o)$$

$$v_{o1} = \frac{v_{od}}{2}$$

$$\therefore \frac{v_{od}}{v_{id}} = -g_m(R_D \parallel r_o)$$

Differential pair acts as CS amplifier for input difference!

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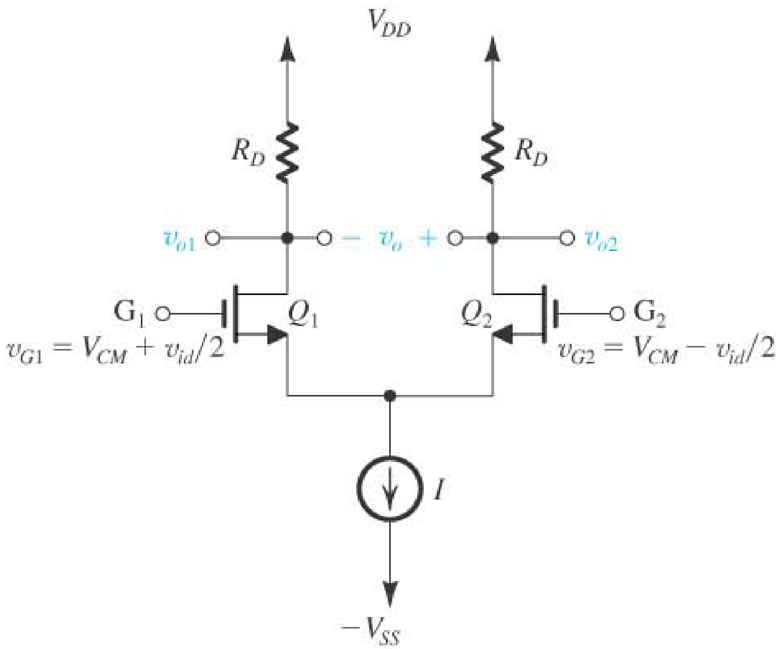


Why a differential amplifier?

- Input stage for operational amplifier (Op-Amp)

- Not sensitive to noises that are common to both input signals.

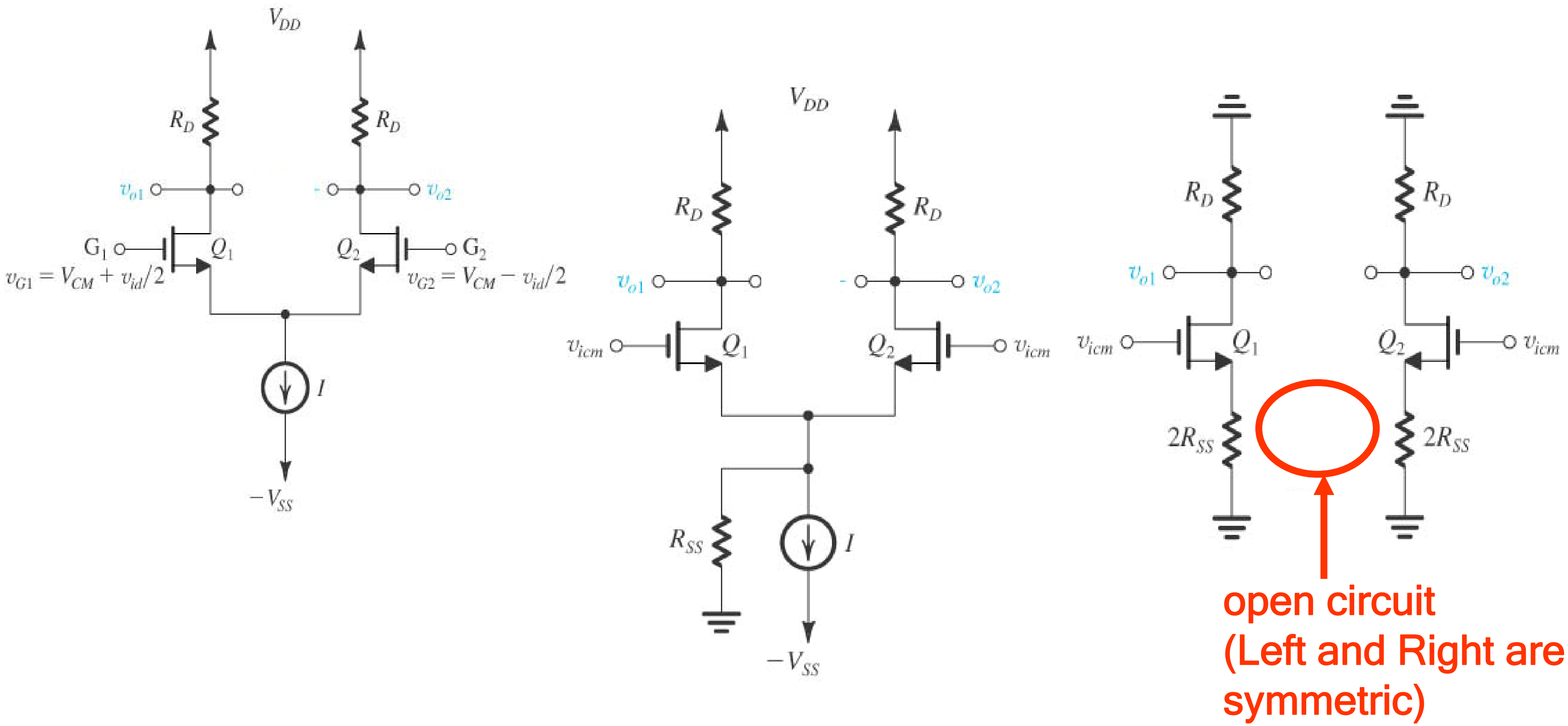
Common-Mode Rejection Ratio

CMRR = $|A_d/A_{cm}|$

Ideally, infinite

What if the current source is NOT ideal?

Common-mode



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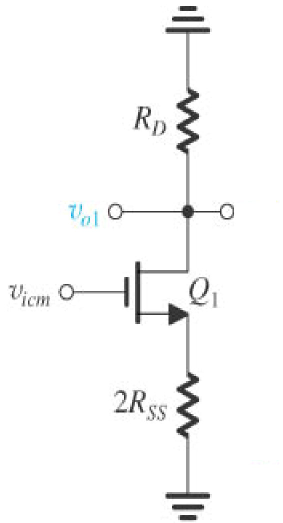
Common-Source with source resistance

Common-mode half circuit



$$\frac{v_{o1}}{v_{icm}} = ? \qquad v_{o1} = -g_m v_{gs} R_D$$

$$v_{gs} = v_{icm} - g_m v_{gs}(2R_{SS})$$

$$v_{gs} = \frac{v_{icm}}{1 + 2g_m R_{SS}}$$

$$\frac{v_{o1}}{v_{icm}} = -\frac{g_m R_D}{1 + 2g_m R_{SS}} \simeq -\frac{R_D}{2R_{SS}}$$

➔ common-mode gain due to R_{ss} for single-ended output

Differential output ($v_o = v_{o1} - v_{o2}$), $v_o = 0$

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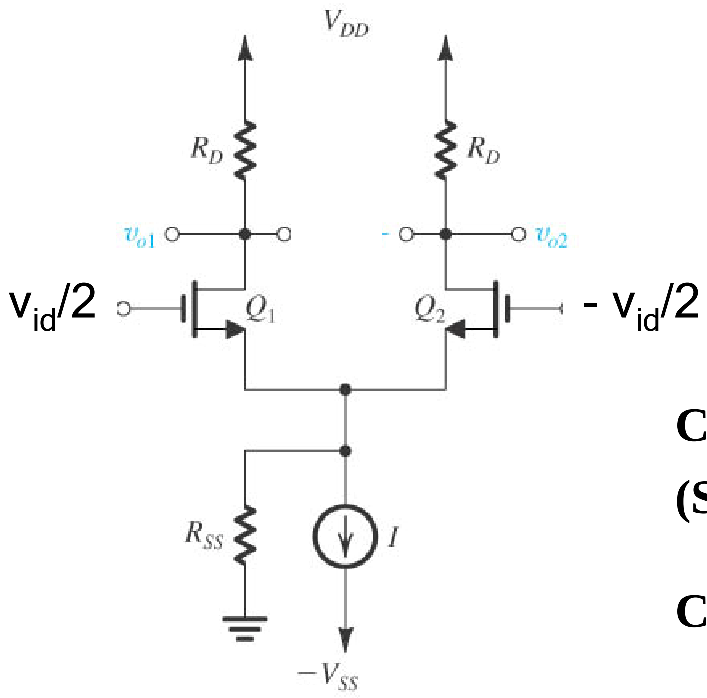
What if the current source is NOT ideal? Differential-Mode



With anti-symmetric input,
the mid-point is still small-signal ground!

$$A_d = -g_m(R_D \| r_o)$$

CMRR: Common-Mode Rejection Ratio

(Single-ended output)

$$\text{CMRR}=\left|\frac{A_d}{A_{cm}}\right| \simeq \frac{g_m(R_D \| r_o)}{\dfrac{R_D}{2R_{ss}}}$$

CMRR for differential output?

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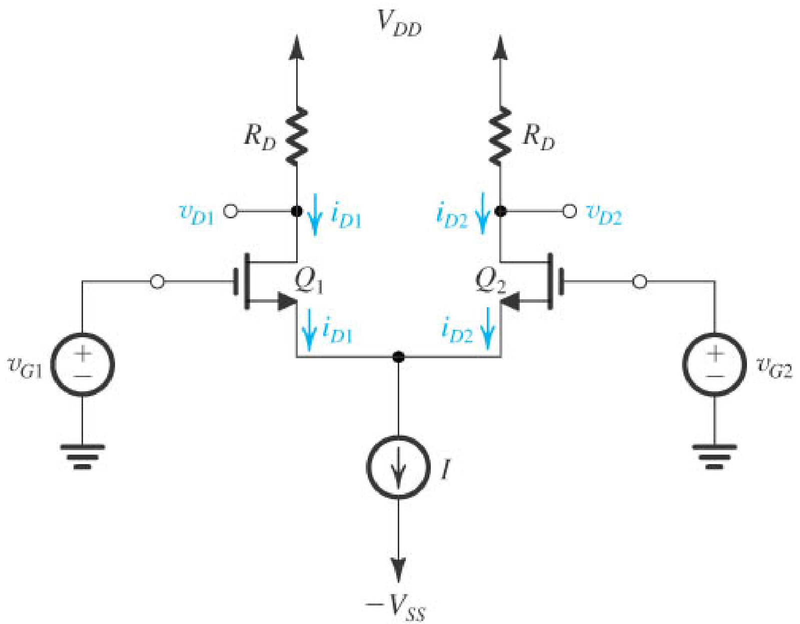

MOS differential pair is based on the symmetry

Anything that breaks the symmetry affects the circuit performance (CMRR, input offset)

Device mismatches cause non-ideal performance → Eliminate R_D

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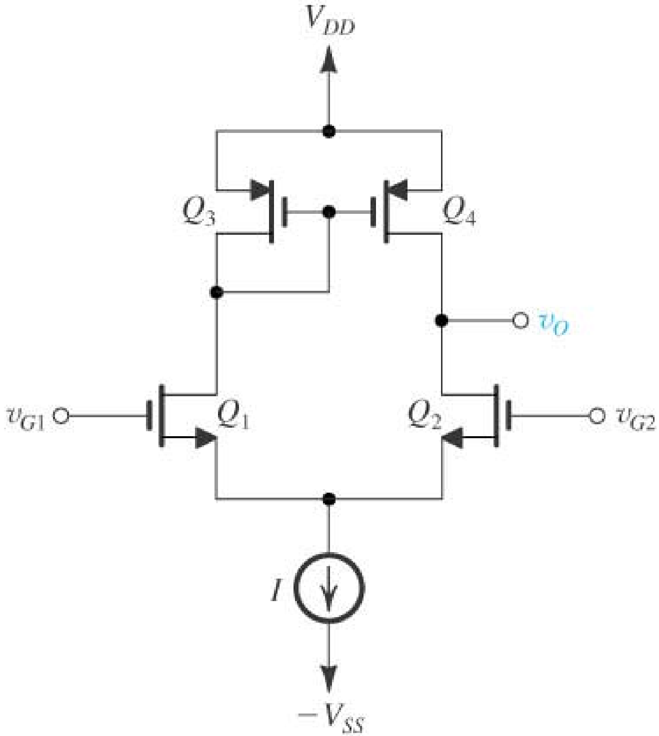
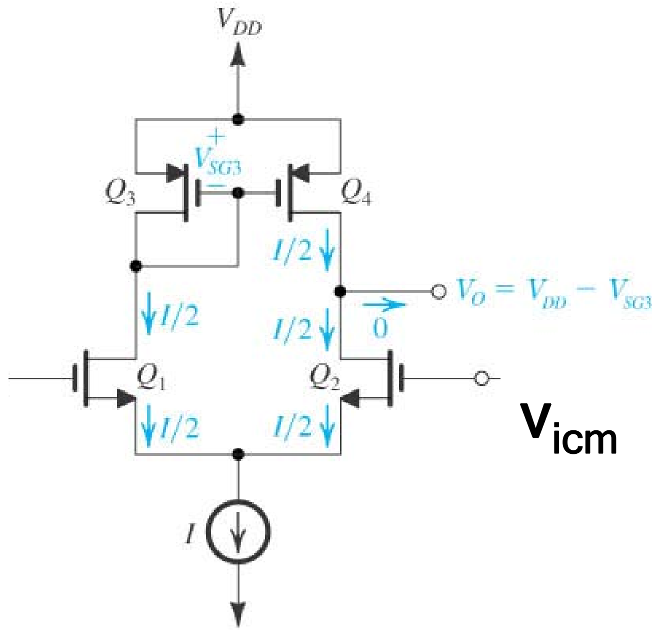
Active-loaded MOS differential pair (single-ended)



V_{icm}



V_{icm}

Common mode

It can be shown with finite R_{ss},

$$A_{cm} = \frac{v_o}{v_{icm}} \simeq -\frac{1}{2 g_m R_{ss}}$$

due to non-ideal current source.

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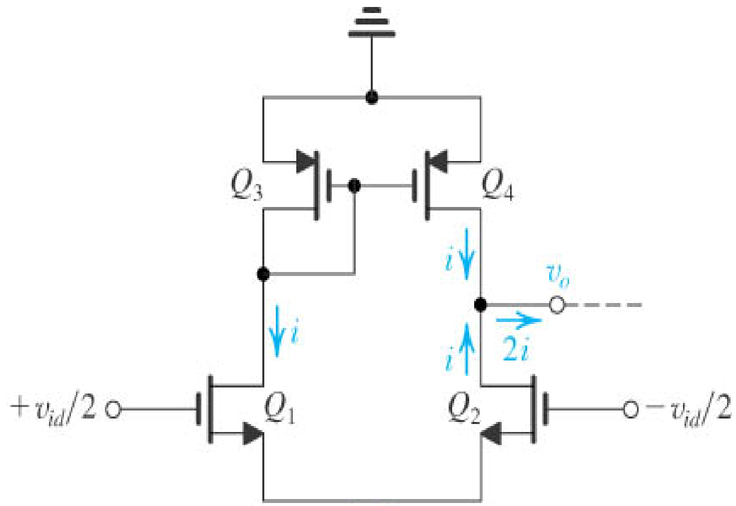
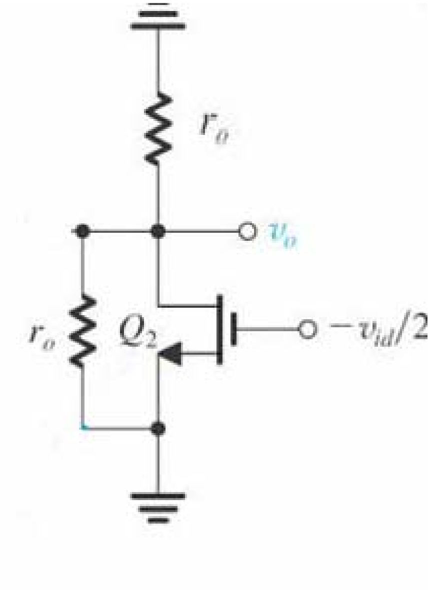
Differential mode small-signal analysis





$$\frac{v_o}{-v_{id}/2} = -g_m(r_o \parallel r_o)$$

$$\therefore \frac{v_o}{v_{id}} = \frac{g_m r_o}{4}$$

Assume it is (almost) symmetric

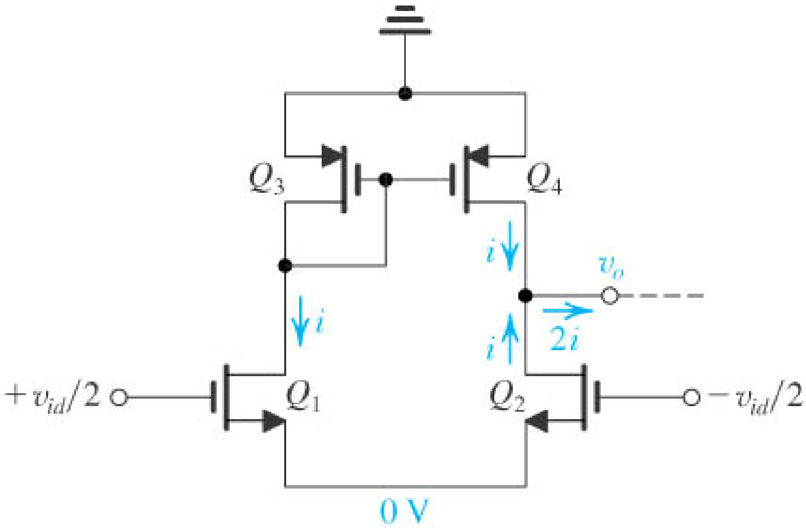
➔ Source terminals are grounded

Half circuit analysis is possible

But with more detailed analysis,

$$A_d = \frac{v_o}{v_{id}} = \frac{g_m r_o}{2}$$

What is wrong with the half-circuit analysis?



The current mirror action is not considered!

Current mirror doubles the transconductance

➔ Twice voltage gain!

$$\therefore A_d = \frac{v_o}{v_{id}} = \frac{1}{2} g_m r_o$$

$$\therefore CMRR = \left| \frac{A_d}{A_{cm}} \right| \simeq \frac{\frac{1}{2} g_m r_o}{\frac{1}{2 g_m R_{ss}}} = g_m{}^2 r_o R_{ss}$$